PC/104+ CPU Board Model 301 (Rev.B)

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Table of Contents

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Special handling instructions

The circuit board contains CMOS circuitry that is sensitive to Electrostatic Discharge (ESD).

Special care should be taken in handling, transporting, and installing circuit board to prevent ESD damage to the board. In particular:

- Do not remove the circuit board from its protective anti-static bag until you are ready to install the board into the enclosure.
- Handle the circuit board only at grounded, ESD protected stations.
- Remove power from the equipment before installing or removing the circuit board.

Introduction

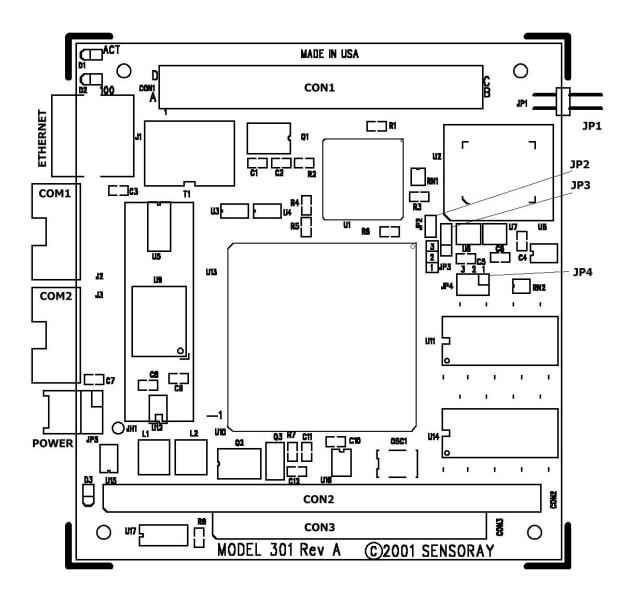
Model 301 is a highly integrated PC/AT compatible CPU board in a PC/104+ format. It is built around AMD Elan SC520 133MHz microcontroller targeted for general embedded market. Model 301 incorporates the features most commonly required in embedded applications, providing the system integrators with a powerful and cost-effective solution.

Feature Summary

- PC/104+ form factor: 3.6 x 3.8 in.
- PC/104 and PC/104+ expansion buses.
- One power source (+5V) operation.
- 32 MB of SDRAM.
- 16 MB flash drive.
- 2 high speed RS-232 ports (1.152 Mbaud).
- 10/100-BaseT(X) Ethernet.
- Watchdog timer.
- Battery-less operation (CMOS configuration data saved in a serial EEPROM).
- Optional DiskOnChip supported.

Reference

Connectors



PC/104+ Expansion Bus Connector, CON1.

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	Ground	B1	n/c	C1	+5 V	D1	AD0
A2	VIO*	B2	AD2	C2	AD1	D2	+5 V
A3	AD5	В3	Ground	C3	AD4	D3	AD3
A4	C/BE0#	B4	AD7	C4	Ground	D4	AD6
A5	Ground	B5	AD9	C5	AD8	D5	Ground
A6	AD11	В6	VIO*	С6	AD10	D6	n/c
A7	AD14	B7	AD13	C7	Ground	D7	AD12
A8	n/c	B8	C/BE1#	C8	AD15	D8	n/c
Α9	SERR#	B9	Ground	С9	SB0	D9	PAR
A10	Ground	B10	PERR#	C10	n/c	D10	SDONE
A11	STOP#	B11	n/c	C11	n/c	D11	Ground
A12	n/c	B12	TRDY#	C12	Ground	D12	DEVSEL#
A13	FRAME#	B13	Ground	C13	IRDY#	D13	n/c
A14	Ground	B14	AD16	C14	n/c	D14	C/BE2#
A15	AD18	B15	n/c	C15	AD17	D15	Ground
A16	AD21	B16	AD20	C16	Ground	D16	AD19
A17	n/c	B17	AD23	C17	AD22	D17	n/c
A18	IDSEL0	B18	Ground	C18	IDSEL1	D18	IDSEL2
A19	AD24	B19	C/BE3#	C19	VIO*	D19	IDSEL3
A20	Ground	B20	AD26	C20	AD25	D20	Ground
A21	AD29	B21	+5 V	C21	AD28	D21	AD27
A22	+5 V	B22	AD30	C22	Ground	D22	AD31
A23	REQ0#	B23	Ground	C23	REQ1#	D23	VIO*
A24	Ground	B24	REQ2#	C24	+5 V	D24	GNT0#
A25	GNT1#	B25	VIO*	C25	GNT2#	D25	Ground
A26	+5 V	B26	CLK0	C26	Ground	D26	CLK1
A27	CLK2	B27	+5 V	C27	CLK3	D27	Ground
A28	Ground	B28	INTD#	C28	+5 V	D28	RST#
A29	+12 V	B29	INTA#	C29	INTB#	D29	INTC#
A30	-12 V	B30	n/c	C30	n/c	D30	Ground

Note:

^{* -} connected to +5 V supply.

PC/104 Expansion Bus Connector AB, CON2.

A1 n/c B1 Ground A2 SD7 B2 RSTDRV A3 SD6 B3 +5 V A4 SD5 B4 IRQ9 A5 SD4 B5 -5 V A6 SD3 B6 DRQ2 A7 SD2 B7 -12 V A8 SD1 B8 n/c A9 SD0 B9 +12 V A10 IOCHRDY B10 n/c A11 AEN B11 n/c A11 AEN B11 n/c A12 SA19 B12 n/c A13 SA18 B13 IOW# A14 SA17 B14 IOR# A14 SA17 B14 IOR# A14 SA15 B16 DRO3 A17 SA14 B17 n/c A18 SA13 B18 n/c A19 SA12 B19	Pin	Signal	Pin	Signal
A3 SD6 B3 +5 V A4 SD5 B4 IRQ9 A5 SD4 B5 -5 V A6 SD3 B6 DRQ2 A7 SD2 B7 -12 V A8 SD1 B8 n/c A9 SD0 B9 +12 V A10 IOCHRDY B10 n/c A11 AEN B11 n/c A11 AEN B11 n/c A12 SA19 B12 n/c A13 SA18 B13 IOW# A14 SA17 B14 IOR# A15 SA16 B15 DACK3# A16 SA15 B16 DR03 A17 SA14 B17 n/c A18 SA13 B18 n/c A19 SA12 B19 REFRESH# A20 SA11 B20 n/c A21 SA10 B21 </td <td>A1</td> <td>n/c</td> <td>B1</td> <td>Ground</td>	A1	n/c	B1	Ground
A4 SD5 B4 IRQ9 A5 SD4 B5 -5 V A6 SD3 B6 DRQ2 A7 SD2 B7 -12 V A8 SD1 B8 n/c A9 SD0 B9 +12 V A10 IOCHRDY B10 n/c A11 AEN B11 n/c A12 SA19 B12 n/c A13 SA18 B13 IOW# A14 SA17 B14 IOR# A15 SA16 B15 DACK3# A16 SA15 B16 DRO3 A17 SA14 B17 n/c A18 SA13 B18 n/c A19 SA12 B19 REFRESH# A20 SA11 B20 n/c A21 SA10 B21 IRO7 A22 SA9 B22 IRQ6 A23 SA8 B2	A2	SD7	B2	RSTDRV
A5 SD4 B5 -5 V A6 SD3 B6 DRQ2 A7 SD2 B7 -12 V A8 SD1 B8 n/c A9 SD0 B9 +12 V A10 IOCHRDY B10 n/c A11 AEN B11 n/c A12 SA19 B12 n/c A13 SA18 B13 IOW# A14 SA17 B14 IOR# A14 SA17 B14 IOR# A15 SA16 B15 DACK3# A16 SA15 B16 DRQ3 A17 SA14 B17 n/c A18 SA13 B18 n/c A19 SA12 B19 REFRESH# A20 SA11 B20 n/c A21 SA10 B21 IRQ7 A22 SA9 B22 IRQ6 A23 SA8 <td< td=""><td>A3</td><td>SD6</td><td>B3</td><td>+5 V</td></td<>	A3	SD6	B3	+5 V
A6 SD3 B6 DRQ2 A7 SD2 B7 -12 V A8 SD1 B8 n/c A9 SD0 B9 +12 V A10 IOCHRDY B10 n/c A11 AEN B11 n/c A11 AEN B11 n/c A12 SA19 B12 n/c A12 SA19 B12 n/c A13 SA18 B13 IOW# A14 SA17 B14 IOR# A15 SA16 B15 DACK3# A16 SA15 B16 DRQ3 A17 SA14 B17 n/c A18 SA13 B18 n/c A19 SA12 B19 REFRESH# A20 SA11 B20 n/c A21 SA10 B21 IRQ7 A22 SA9 B22 IRQ6 A23 SA8 <td< td=""><td>A4</td><td>SD5</td><td>B4</td><td>IRQ9</td></td<>	A4	SD5	B4	IRQ9
A7 SD2 B7 -12 V A8 SD1 B8 n/c A9 SD0 B9 +12 V A10 IOCHRDY B10 n/c A11 AEN B11 n/c A11 AEN B11 n/c A12 SA19 B12 n/c A12 SA19 B12 n/c A13 SA18 B13 IOW# A14 SA17 B14 IOR# A14 SA17 B14 IOR# A15 SA16 B15 DACK3# A16 SA15 B16 DRQ3 A17 SA14 B17 n/c A18 SA13 B18 n/c A19 SA12 B19 REFRESH# A20 SA11 B20 n/c A21 SA10 B21 IRQ7 A22 SA9 B22 IRQ6 A23 SA8	A5	SD4	B5	-5 V
A8 SD1 B8 n/c A9 SD0 B9 +12 V A10 IOCHRDY B10 n/c A11 AEN B11 n/c A12 SA19 B12 n/c A13 SA18 B13 IOW# A14 SA17 B14 IOR# A15 SA16 B15 DACK3# A15 SA16 B15 DACK3# A16 SA15 B16 DRQ3 A17 SA14 B17 n/c A18 SA13 B18 n/c A19 SA12 B19 REFRESH# A20 SA11 B20 n/c A21 SA10 B21 IRQ7 A22 SA9 B22 IRQ6 A23 SA8 B23 IRQ6 A24 SA7 B24 IRQ4 A25 SA6 B25 IRQ3 A26 SA5	A6	SD3	B6	DRQ2
A9 SD0 B9 +12 V A10 IOCHRDY B10 n/c A11 AEN B11 n/c A12 SA19 B12 n/c A13 SA18 B13 IOW# A14 SA17 B14 IOR# A15 SA16 B15 DACK3# A15 SA16 B15 DACK3# A16 SA15 B16 DRQ3 A17 SA14 B17 n/c A18 SA13 B18 n/c A19 SA12 B19 REFRESH# A20 SA11 B20 n/c A21 SA10 B21 IRQ7 A22 SA9 B22 IRQ6 A23 SA8 B23 IRQ5 A24 SA7 B24 IRQ4 A25 SA6 B25 IRQ3 A26 SA5 B26 DACK2# A27 SA4	A7	SD2	В7	-12 V
A10 IOCHRDY B10 n/c A11 AEN B11 n/c A12 SA19 B12 n/c A13 SA18 B13 IOW# A14 SA17 B14 IOR# A15 SA16 B15 DACK3# A16 SA15 B16 DRQ3 A17 SA14 B17 n/c A18 SA13 B18 n/c A19 SA12 B19 REFRESH# A20 SA11 B20 n/c A21 SA10 B21 IRQ7 A22 SA9 B22 IRQ6 A23 SA8 B23 IRQ5 A24 SA7 B24 IRQ4 A25 SA6 B25 IRQ3 A26 SA5 B26 DACK2# A27 SA4 B27 TC A28 SA3 B28 BALE A29 SA2	A8	SD1	B8	n/c
A11 AEN B11 n/c A12 SA19 B12 n/c A13 SA18 B13 IOW# A14 SA17 B14 IOR# A15 SA16 B15 DACK3# A16 SA15 B16 DRQ3 A17 SA14 B17 n/c A18 SA13 B18 n/c A19 SA12 B19 REFRESH# A20 SA11 B20 n/c A21 SA10 B21 IRQ7 A22 SA9 B22 IRQ6 A23 SA8 B23 IRQ5 A24 SA7 B24 IRQ4 A25 SA6 B25 IRQ3 A26 SA5 B26 DACK2# A27 SA4 B27 TC A28 SA3 B28 BALE A29 SA2 B29 +5 V A30 SA1	А9	SD0	В9	+12 V
A12 SA19 B12 n/c A13 SA18 B13 IOW# A14 SA17 B14 IOR# A15 SA16 B15 DACK3# A16 SA15 B16 DRQ3 A17 SA14 B17 n/c A18 SA13 B18 n/c A19 SA12 B19 REFRESH# A20 SA11 B20 n/c A21 SA10 B21 IRQ7 A22 SA9 B22 IRQ6 A23 SA8 B23 IRQ5 A24 SA7 B24 IRQ4 A25 SA6 B25 IRQ3 A26 SA5 B26 DACK2# A27 SA4 B27 TC A28 SA3 B28 BALE A29 SA2 B29 +5 V A30 SA1 B30 OSC A31 SA0	A10	IOCHRDY	B10	n/c
A13 SA18 B13 IOW# A14 SA17 B14 IOR# A15 SA16 B15 DACK3# A16 SA15 B16 DRQ3 A17 SA14 B17 n/c A18 SA13 B18 n/c A19 SA12 B19 REFRESH# A20 SA11 B20 n/c A21 SA10 B21 IRQ7 A22 SA9 B22 IRQ6 A23 SA8 B23 IRQ5 A24 SA7 B24 IRQ4 A25 SA6 B25 IRQ3 A26 SA5 B26 DACK2# A27 SA4 B27 TC A28 SA3 B28 BALE A29 SA2 B29 +5 V A30 SA1 B30 OSC A31 SA0 B31 Ground	A11	AEN	B11	n/c
A14 SA17 B14 IOR# A15 SA16 B15 DACK3# A16 SA15 B16 DRO3 A17 SA14 B17 n/c A18 SA13 B18 n/c A19 SA12 B19 REFRESH# A20 SA11 B20 n/c A21 SA10 B21 IRQ7 A22 SA9 B22 IRQ6 A23 SA8 B23 IRQ5 A24 SA7 B24 IRQ4 A25 SA6 B25 IRQ3 A26 SA5 B26 DACK2# A27 SA4 B27 TC A28 SA3 B28 BALE A29 SA2 B29 +5 V A30 SA1 B30 OSC A31 SA0 B31 Ground	A12	SA19	B12	n/c
A15 SA16 B15 DACK3# A16 SA15 B16 DRQ3 A17 SA14 B17 n/c A18 SA13 B18 n/c A19 SA12 B19 REFRESH# A20 SA11 B20 n/c A21 SA10 B21 IRQ7 A22 SA9 B22 IRQ6 A23 SA8 B23 IRQ5 A24 SA7 B24 IRQ4 A25 SA6 B25 IRQ3 A26 SA5 B26 DACK2# A27 SA4 B27 TC A28 SA3 B28 BALE A29 SA2 B29 +5 V A30 SA1 B30 OSC A31 SA0 B31 Ground	A13	SA18	B13	IOW#
A16 SA15 B16 DRQ3 A17 SA14 B17 n/c A18 SA13 B18 n/c A19 SA12 B19 REFRESH# A20 SA11 B20 n/c A21 SA10 B21 IRQ7 A22 SA9 B22 IRQ6 A23 SA8 B23 IRQ5 A24 SA7 B24 IRQ4 A25 SA6 B25 IRQ3 A26 SA5 B26 DACK2# A27 SA4 B27 TC A28 SA3 B28 BALE A29 SA2 B29 +5 V A30 SA1 B30 OSC A31 SA0 B31 Ground	A14	SA17	B14	IOR#
A17 SA14 B17 n/c A18 SA13 B18 n/c A19 SA12 B19 REFRESH# A20 SA11 B20 n/c A21 SA10 B21 IRQ7 A22 SA9 B22 IRQ6 A23 SA8 B23 IRQ5 A24 SA7 B24 IRQ4 A25 SA6 B25 IRQ3 A26 SA5 B26 DACK2# A27 SA4 B27 TC A28 SA3 B28 BALE A29 SA2 B29 +5 V A30 SA1 B30 OSC A31 SA0 B31 Ground	A15	SA16	B15	DACK3#
A18 SA13 B18 n/c A19 SA12 B19 REFRESH# A20 SA11 B20 n/c A21 SA10 B21 IRQ7 A22 SA9 B22 IRQ6 A23 SA8 B23 IRQ5 A24 SA7 B24 IRQ4 A25 SA6 B25 IRQ3 A26 SA5 B26 DACK2# A27 SA4 B27 TC A28 SA3 B28 BALE A29 SA2 B29 +5 V A30 SA1 B30 OSC A31 SA0 B31 Ground	A16	SA15	B16	DRQ3
A19 SA12 B19 REFRESH# A20 SA11 B20 n/c A21 SA10 B21 IRQ7 A22 SA9 B22 IRQ6 A23 SA8 B23 IRQ5 A24 SA7 B24 IRQ4 A25 SA6 B25 IRQ3 A26 SA5 B26 DACK2# A27 SA4 B27 TC A28 SA3 B28 BALE A29 SA2 B29 +5 V A30 SA1 B30 OSC A31 SA0 B31 Ground	A17	SA14	B17	n/c
A20 SA11 B20 n/c A21 SA10 B21 IRQ7 A22 SA9 B22 IRQ6 A23 SA8 B23 IRQ5 A24 SA7 B24 IRQ4 A25 SA6 B25 IRQ3 A26 SA5 B26 DACK2# A27 SA4 B27 TC A28 SA3 B28 BALE A29 SA2 B29 +5 V A30 SA1 B30 OSC A31 SA0 B31 Ground	A18	SA13	B18	n/c
A21 SA10 B21 IRQ7 A22 SA9 B22 IRQ6 A23 SA8 B23 IRQ5 A24 SA7 B24 IRQ4 A25 SA6 B25 IRQ3 A26 SA5 B26 DACK2# A27 SA4 B27 TC A28 SA3 B28 BALE A29 SA2 B29 +5 V A30 SA1 B30 OSC A31 SA0 B31 Ground	A19	SA12	B19	REFRESH#
A22 SA9 B22 IRQ6 A23 SA8 B23 IRQ5 A24 SA7 B24 IRQ4 A25 SA6 B25 IRQ3 A26 SA5 B26 DACK2# A27 SA4 B27 TC A28 SA3 B28 BALE A29 SA2 B29 +5 V A30 SA1 B30 OSC A31 SA0 B31 Ground	A20	SA11	B20	n/c
A23 SA8 B23 IRQ5 A24 SA7 B24 IRQ4 A25 SA6 B25 IRQ3 A26 SA5 B26 DACK2# A27 SA4 B27 TC A28 SA3 B28 BALE A29 SA2 B29 +5 V A30 SA1 B30 OSC A31 SA0 B31 Ground	A21	SA10	B21	IRQ7
A24 SA7 B24 IRQ4 A25 SA6 B25 IRQ3 A26 SA5 B26 DACK2# A27 SA4 B27 TC A28 SA3 B28 BALE A29 SA2 B29 +5 V A30 SA1 B30 OSC A31 SA0 B31 Ground	A22	SA9	B22	IRQ6
A25 SA6 B25 IRQ3 A26 SA5 B26 DACK2# A27 SA4 B27 TC A28 SA3 B28 BALE A29 SA2 B29 +5 V A30 SA1 B30 OSC A31 SA0 B31 Ground	A23	SA8	B23	IRQ5
A26 SA5 B26 DACK2# A27 SA4 B27 TC A28 SA3 B28 BALE A29 SA2 B29 +5 V A30 SA1 B30 OSC A31 SA0 B31 Ground	A24	SA7	B24	IRQ4
A27 SA4 B27 TC A28 SA3 B28 BALE A29 SA2 B29 +5 V A30 SA1 B30 OSC A31 SA0 B31 Ground	A25	SA6	B25	IRQ3
A28 SA3 B28 BALE A29 SA2 B29 +5 V A30 SA1 B30 OSC A31 SA0 B31 Ground	A26	SA5	B26	DACK2#
A29 SA2 B29 +5 V A30 SA1 B30 OSC A31 SA0 B31 Ground	A27	SA4	B27	TC
A30 SA1 B30 OSC A31 SA0 B31 Ground	A28	SA3	B28	BALE
A31 SA0 B31 Ground	A29	SA2	B29	+5 V
	A30	SA1	B30	OSC
A32 Ground B32 Ground	A31	SA0	B31	Ground
	A32	Ground	B32	Ground

PC/104 Expansion Bus Connector CD, CON3.

Pin	Signal	Pin	Signal
CO	Ground	D0	Ground
C1	SBHE#	D1	MEMCS16#
C2	LA23	D2	IOCS16#
C3	LA22	D3	IRQ10
C4	LA21	D4	IRQ11
C5	LA20	D5	IRQ12
C6	LA19	D6	IRQ15
C7	LA18	D7	IRQ14
C8	LA17	D8	n/c
С9	MEMR#	D9	n/c
C10	MEMW#	D10	DACK5#
C11	SD8	D11	DRQ5
C12	SD9	D12	DACK6#
C13	SD10	D13	DRQ6
C14	SD11	D14	DACK7#
C15	SD12	D15	DRQ7
C16	SD13	D16	+5 V
C17	SD14	D17	n/c
C18	SD15	D18	Ground
C19	n/c	D19	Ground

Serial ports (COM1, COM2) connectors, J2, J3.

Pin	Signal	Pin	Signal
1	DCD	2	DSR
3	RXD	4	RTS
5	TXD	6	CTS
7	DTR	8	RI
9	Ground	10	n/c

Power connector, JP5.

The power connector is Hirose DF11-6DP-2DS22. The mating connector is Hirose DF11-6DS-2C.

Pin	Signal	Pin	Signal
1	+5 V	2	Ground
3	+12 V	4	-5 V
5	-12 V	6	Ground

Note:

Only +5 V power supply is required for operation. Other pins of the power connector are connected only to the corresponding pins of the PC/104 and PC/104+ connectors.

Reset connector, JP1.

Pin	Signal	Pin	Signal
1	Manual reset	2	Ground
3	Open collector	4	Ground

See Watchdog Timer section for the description of reset connector signals.

Ethernet connector, J1.

The Ethernet connector is a right-angle 8-pin RJ-45.

Pin	Signal	
1	TX+	
2	TX-	
3	RX+	
7	RX-	

Configuration jumpers

Watchdog timer reset, JP2.

If this jumper is inserted, the watchdog timer reset signal is connected to the CPU reset. Otherwise the CPU is not reset by the watchdog timer reset signal.

Open collector default state, JP3.

The watchdog timer reset signal drives a transistor with an open collector output connected to connector JP1. The default state of the open collector output (open or closed) is selected by the jumper JP3. The jumper in the position 1-2 results in normally closed output (driven low), which switches to open (driven high) during the watchdog timer reset. The jumper in the position 2-3 results in normally open output (driven high), which switches to closed (driven low) during the watchdog timer reset. The board is shipped with this jumper in the position 1-2.

System configuration, JP4.

System configuration jumpers JP4-1, JP4-2, and JP4-3 are used to select special operating modes of model 301.

Inserting the jumper JP4-2 causes the CPU to go directly into the setup screen after being powered up or reset. This allows accessing the setup screen even when the system is configured to boot as fast as possible, in which case the usual method of setup screen access (hitting the Delete key during the Power On Self Test) may be hard to use.

The jumpers in positions JP4-1 and JP4-3 are reserved for testing and future use. The board is shipped without any of these jumpers installed.

CPU resources usage

System memory

The 301 has 16 Mbytes of RAM installed at the factory.

Address range	Function
000000h-09FFFFh	Lower 640 Kbytes
0A0000h-0BFFFFh	Video RAM (if video adapter is installed)
0C0000h-0CBFFFh	Video BIOS (if video adapter is installed)
0CC000h-0CDFFFh	DiskOnChip 8 Kbyte window
0CE000h-0CFFFFh	Free
0D0000h-0D7FFFh	Mapped to ISA bus memory access
0D8000h-0DEFFFh	Mapped to PCI bus memory access
0DF000h-0DFFFFh	Free
0E0000h-0FFFFh	BIOS
100000h-FFFFFh	Extended memory

System I/O addresses

The I/O accesses are routed to internal peripherals, on-board devices, or extension buses according to the following table.

I/O address range	Function	
0000h-000Fh	Slave ISA DMA controller	
001Eh-001Fh	Watchdog timer	
0020h-0021h	Master interrupt controller	
0024h-0025h	Reserved	
0040h-0043h	Reserved	
0060h-0064h	Reserved	
0070h-0071h	Real time clock	
0080h, 0084h-0086h,0088h,008Ch-008Eh	General purpose scratch registers (writes to those addresses are also seen on the ISA bus)	
008Fh	General purpose scratch register (writes to this register are not seen on the ISA bus)	
0081h-0083h,0087h,0089h-008Bh	ISA DMA page registers	
0092h	System control port A	
00A0h-00A1h	Slave 1 interrupt controller	
00C0h-00DEh	Master ISA DMA controller	
00F0h	Floating point error interrupt clear	
02F8h-02FFh	Internal UART2	
03F8h-03FFh	Internal UART1	
0400h-09FFh	Mapped to ISA bus I/O access	

Note:

 $\mbox{I/O}$ accesses to the addresses not listed in the table are routed to PCI bus, except for the case when an ISA VGA card is used, in which case they are routed to ISA bus.

Setup

Some of the features of model 301 are controlled through the Setup screens (similar to desktop PC's). The configuration settings are stored in the EEPROM, so that the board does not require a battery to retain the configuration. The real-time clock, however, requires a battery to keep running when the power is turned off. A battery holder is provided on the back side of the board to accommodate an optional 3 Volt 20mm battery (e.g. Panasonic CR2032).

The Setup consists of 3 screens: Basic CMOS Configuration, Custom Configuration, and Flash Disk Format.

The Basic CMOS Configuration Screen contains the settings typical to most PC's.

The Custom Configuration Screen contains the following settings:

- 1. "ISA Timing" controls the speed if the ISA bus. The following selections are available:
 - SLOW (default) standard ISA timing (8 MHz clock);
 - MEDIUM approximately 10 MHz ISA clock;
 - FAST 12 MHz ISA clock.
- 2. "COM3 (uses IRQ10)" enables/disables serial port COM3 on model 300TA PC I/O board. This port is configured to use interrupt line IRQ10. In case this line has to be used by other add-on boards, the serial port has to be disabled.
- 3. "COM4 (uses IRQ11)" enables/disables serial port COM4 on model 300TA PC I/O board. This port is configured to use interrupt line IRQ11. In case this line has to be used by other add-on boards, the serial port has to be disabled.
- 4. "LPT1 (uses IRQ7)" enables/disables parallel port LPT1 on model 300TA PC I/O board. This port is configured to use interrupt line IRQ7. In case this line has to be used by other add-on boards, the parallel port has to be disabled.
- 5. "IDE1 (uses IRQ14)" enables/disables IDE channel 1 on model 300TA PC I/O board. This channel is configured to use interrupt line IRQ14. In case this line has to be used by other add-on boards, the IDE channel 1 has to be disabled.
- 6. "IDE2 (uses IRQ15)" enables/disables IDE channel 2 on model 300TA PC I/O board. This channel is configured to use interrupt line IRQ15. In case this line has to be used by other add-on boards, the IDE channel 2 has to be disabled.

The Flash Disk Format Screen allows formatting of the integrated 8 MB flash disk. Model 301 is shipped with the flash disk already formatted.

Serial ports

Two high speed (300 baud to 1.152 Mbaud) serial ports are integrated on model 301. They have standard resources assignment:

COM1: base address 2F8h, interrupt line IRQ4;

COM2: base address 3F8h, interrupt line IRQ3.

Ethernet

Model 301 incorporates the integrated Ethernet adapter based on Intel GD82559ER Fast Ethernet PCI Controller. The controller complies with IEEE802.3 10BASE-T and 100BASE-TX specifications and supports full duplex mode at both 10 and 100 Mbps.

A standard RJ-45 connector is provided on model 301 for connecting to the twisted-pair line. Two LED's provide an indication of the operating mode: D1 indicates line activity, and D2 indicates 100 Mbps network (when on).

The Ethernet controller uses the INTD# interrupt line of the PC/104+ expansion bus. No add-on device should use the same interrupt line.

Drivers for various operating systems are available from Intel's Web site: http://developer.intel.com/design/network/drivers/index.htm#82559

DiskOnChip Support

Model 301 supports an optional M-Systems DiskOnChip (a flash device emulating a hard drive). A socket is provided to accommodate a 32-pin DIP package. **Model 301 supports 3 Volt parts only.**

DiskOnChip contains an internal BIOS extension that allows it to be detected by an operating system without having to configure the setup settings. It may be set up to appear as the first or the last drive in the system. Please refer to the M-Systems documentation for the details.

Specifications

CPU	AMD SC520 133 MHz
RAM	16 MB
Expansion buses	PC/104, PC/104+
Interrupts	15 channels (8 channels available for add-on
·	boards)
DMA (ISA)	4 channels
Flash disk	8 MB
Disk-On-Chip	supported as an option
Watchdog timer	1.6 s timeout, configurable to reset the CPU
	and/or drive the open collector output with
	programmable default state
Serial ports	Two 16550-compatible UARTs, 300 baud –
	1.152 Mbaud, RS-232
Ethernet	10/100Base-T(X), Intel GD82559ER PCI
	controller
Power	+5 V, 1A

PC I/O board model 300TA

Model 300TA is a PC/104 board that provides a set of standard PC peripherals for model 301 CPU board:

- 2 IDE channels for up to 4 devices;
- Floppy interface;
- 2 serial ports;
- 1 parallel port;
- Keyboard and mouse ports.

Connectors

Standard connectors

The following peripherals are provided with standard connectors on model 300TA: IDE channels 1 and 2, floppy, keyboard, mouse. The pinout for those connectors can be found in the PC documentation.

Parallel port connector, LPT.

Pin	Signal	Pin	Signal
1	STB#	2	ALF#
3	PD0	4	ERROR#
5	PD1	6	INIT#
7	PD2	8	SLCTIN#
9	PD3	10	Ground
11	PD4	12	Ground
13	PD5	14	Ground
15	PD6	16	Ground
17	PD7	18	Ground
19	ACK#	20	Ground
21	BUSY	22	Ground
23	PE	24	Ground
25	SLCT	26	n/c

Serial ports (COM3, COM4) connectors, J2, J1.

Pin	Signal	Pin	Signal
1	DCD	2	DSR
3	RXD	4	RTS
5	TXD	6	CTS
7	DTR	8	RI
9	Ground	10	n/c

Note:

Connectors J1 and J2 are positioned with pin 1 facing the opposite direction as compared to the serial port connectors on model 301. The same cable can be used for both boards, but care should be taken to insert the connector properly in each case.

Configuration jumpers

Base address, JP1.

Selects the board's base address. Jumper in position 1 corresponds to base address 370h, jumper in position 2 (default) corresponds to base address 3F0h.

DMA, JP2.

Inserting the jumpers connects DMA request and acknowledge lines of the 300TA's peripherals to the PC/104 connector. Removing the jumpers allows those lines to be used by other PC/104 add-on boards. The board ships with the jumpers removed.

Jumper	Signal	PC/104 line
1	LPT DMA request	DREQ3
2	LPT DMA acknowledge	DACK3#
3	IDE2 DMA request	DREQ6
4	IDE2 DMA acknowledge	DACK6#
5	IDE1 DMA request	DREQ5
6	IDE1 DMA acknowledge	DACK5#

IDE

Model 300TA provides an interface to up to 4 IDE peripheral devices, such as hard drives or CD-ROM drives, through 2 standard IDE cable 40-pin connectors (IDE1 and IDE2). An LED (D1) indicates hard drive activity.

The resources assignment for the IDE channels:

IDE1 – base address 1F0h, interrupt line IRQ14, DMA channel 2;

IDE2 – base address 170h, interrupt line IRQ15, DMA channel 3.

Floppy Disk Controller

The Floppy Disk Controller (FDC) is IBM PC XT/AT compatible.

The following resources are used by the FDC: base address 3F0h, interrupt line IRQ6, DMA channel 0.

Parallel Port

Model 300TA incorporates an IBM PC XT/AT compatible parallel port (LPT).

The following resources are used by the LPT: base address 378h, interrupt line IRQ7, DMA channel 1.

Serial Ports

Two high speed (300 baud to 460.8 Kbaud) serial ports are integrated on model 300TA. They have the following resources assignment:

COM3: base address 3E8h, interrupt line IRQ10;

COM4: base address 2E8h, interrupt line IRQ11.

Serial ports COM3 and COM4 can be enabled or disabled through the model 301's setup screen. The resources of the disabled port(s) could be used by other add-on boards.

Keyboard and Mouse

Model 300TA provides standard 8042-compatible keyboard and PS/2 mouse interfaces. The connectors are standard 6-pin mini-DINs.

Because the standard keyboard interrupt line IRQ1 is not present on the PC/104 connector, model 300TA uses interrupt line IRQ5 for keyboard interrupts.